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Semicond. Sci. Technol. **27** (2012) 035020 (7pp) doi:10.1088/0268-1242/27/3/035020

Low interface trapped charge density in MBE *in situ* grown Si_3N_4 cubic GaN MIS structures

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Received 21 November 2011, in final form 11 January 2012
Published 3 February 2012
Online at stacks.iop.org/SST/27/035020

Abstract
In this work we report on the electrical characterization of nonpolar cubic GaN metal–insulator–semiconductor (MIS) structures. Si_3N_4 layers were deposited *in situ* on top of cubic GaN grown on 3C–SiC (0 0 1) substrates. The electric characteristics of the MIS structures are determined by current–voltage measurements and by capacitance and admittance spectroscopy techniques. Time-of-flight secondary ion mass spectroscopy (TOF-SIMS) was used to investigate the composition of our samples. From the flat band voltage in the MIS capacitors and a detailed band diagram analysis, the conduction band discontinuity of Si_3N_4 and cubic GaN was evaluated 1.17 eV, which is slightly lower than reported for hexagonal GaN. By admittance spectroscopy interface state densities are calculated. Current–voltage characteristics were used to evaluate the influence of the substrate temperature on the insulating properties of the MIS structures. The energetic position of the interface traps was found to be about 0.3 eV below the conduction band of cubic GaN. The density of these traps is 2.5×10^{11} cm^{-2} eV^{-1}. We find a conductivity minimum in the MIS structure grown at 600 °C.

(Some figures may appear in colour only in the online journal)

1. Introduction

Recently, the first hetero junction field-effect transistor (HFET) with normally off characteristics based on cubic AlGaN/GaN heterostructure [1] was realized. However, the critical issue in the operation of this device was its high gate leakage current, which is undesirable for high power and low noise applications and severely reduces the device performance. Therefore, the use of metal/insulator layers instead of a Schottky gate, leading to the metal–insulator–semiconductor heterojunction field-effect transistors (MIS-HFET), is proposed for improved device characteristics [2, 3].

Over the years, various insulator materials such as SiO_2, SiO_xN and Si_3N_4 for III–V compounds have been widely studied. These insulators are mainly deposited by plasma-enhanced chemical vapor deposition (PECVD) [4, 5]. However, during transport to the PECVD chamber the c-GaN surface is exposed to the atmosphere, which may lead to the formation of additional defect states. Sufficient high quality of the interface between the insulator and nitride epilayer, however, is one critical issue of any MIS structure. Growing Si_3N_4 *in situ*—directly in the MBE chamber after the growth of c-GaN—may prevent the formation of such defect states.

In section 2 the experimental part of this work is described. Section 3 is divided into two main parts. In the first part the results of capacitance and conduction measurements are discussed. The results are compared with Si_3N_4 and SiO_2 layers produced *ex situ* by the PECVD process. The second part deals with the influence of the substrate temperature on the composition of the Si_3N_4 layers and the influence on their insulating properties. Section 4 concludes the paper.

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2. Experiments

The optimum conditions for the growth of cubic GaN are mainly determined by two parameters, namely the surface stoichiometry and the substrate temperature [7]. Both parameters are interrelated; therefore an *in situ* control of both is necessary. This is achieved by monitoring the growth process by reflection high energy electron diffraction (RHEED). 600 nm thick cubic GaN buffer layers were grown at 720 °C on free standing, highly n-doped 3C–SiC (0 0 1) substrates; the growth rate was 150 nm h^{-1}. Unintentionally doped cubic GaN layers have a background donor concentration of 1×10^{17} cm^{-3}. In order to minimize hexagonal inclusions in our layers and to obtain an optimum interface roughness a coverage of 1 monolayer Ga was established during growth [8, 9].

In our experiments two kinds of sample structures were investigated. In the first series the 600 nm thick c-GaN layers were taken out from the MBE chamber and Si_3N_4 and SiO_2 layers were deposited by plasma-enhanced chemical vapor deposition (PECVD) at a substrate temperature of 300 °C. The deposited insulator thickness was estimated from the saturation region of the CV curves assuming a dielectric constant of 7.5 for Si_3N_4 and 3.9 for SiO_2 [10]. In the second series Si_3N_4 layers were deposited *in situ* in the MBE chamber directly after the growth of the c-GaN buffer using the nitrogen plasma source and the silicon thermal evaporation source. The growth temperature of the Si_3N_4 layers varied between 300 °C and 700 °C. The growth rate which was between 13 nm h^{-1} and 15 nm h^{-1} was estimated from CV characteristics. The background pressure during growth was 7×10^{-6} mbar and the atomic fluxes of atomic nitrogen and silicon were 2×10^{14} $cm^{-2}s^{-1}$ and 1.8×10^{15} cm^{-2} s^{-1}, respectively. Using standard lithography circular contact structures with a diameter of 100 μm were placed on top of the insulating layer. Metal gate contacts were thermally evaporated consisting of 15 nm Ni and 50 nm Au. The ohmic back contacts were realized by soldering the highly conductive 3C–SiC on Cu plates with In. Current–voltage measurements were done with an Agilent Precision Semiconductor Parameter Analyzer 4156C. The MIS capacitors were characterized by means of CV and G–ω measurements using an Agilent Precision E4980A LCR meter. The dc bias varied from deep depletion to accumulation and back to deep depletion. An ac amplitude of 50 mV was used and the measurements were performed under light-tight and electrically shielded environment. Interface trap density values D_{it} have been extracted by admittance spectroscopy. For TOF-SIMS a pulsed 15 keV Ga^+ ion analysis beam and a pulsed 0.5 keV Cs^+ erosion beam were used. To avoid sample charging a pulsed electron shower was used. The negative ion mass spectrum was measured. From these data a depth profile was made for selected, representative signals.

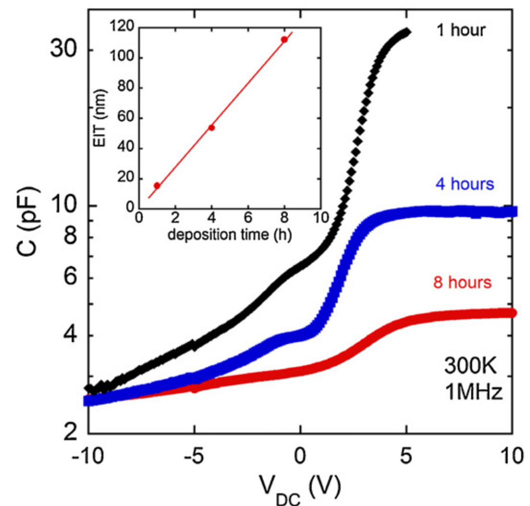

Figure 1. Measured capacitance of the Si_3N_4/c-GaN capacitors versus the applied dc voltage. Three samples were grown at a temperature of 300 °C; the deposition time varied from 1 h to 8 h. The inset shows the linear function of the equivalent insulator thickness as a function of the deposition time. The growth rate is 13.9 nm h^{-1}.

3. Results and discussions

3.1. Interface trapped charge density in MBE grown Si_3N_4/c-GaN MIS structures

Typical CV curves of cubic GaN MIS structures measured at 1 MHz are shown in figure 1. The bias voltage varied from deep depletion (−10 V) to accumulation (+10 V). The accumulation capacitance was used to determine the equivalent insulator thickness (EIT) assuming a dielectric constant of 7.5 for Si_3N_4. The EIT of the MBE-produced Si_3N_4 layers as a function of the deposition time is shown in the inset of figure 1. The thickness of the silicon nitride layers increases linearly with the deposition time. From the slope of the linear fit a growth rate of about 13.9 nm h^{-1} was estimated.

For negative bias voltages no inversion capacitance is observed. With decreasing voltage the capacitance drops and does not saturate. This deep depletion feature is typical for wide band gap semiconductor MIS structures, because the generation rate of the minority carriers (holes) is extremely low at room temperature. Due to the large time constant resulting from an extremely low generation rate of holes the electron quasi-Fermi level will remain unchanged.

Using equation (1) the net donor concentration was calculated from the capacitance–voltage characteristics for each structure:

$$N_D - N_A = -\frac{1}{e\varepsilon_0\varepsilon_r A^2 \left(\mathrm{d}C^{-2}/\mathrm{d}V\right)}. \tag{1}$$

The flat band voltage in the cubic GaN for each of the structures was derived from the donor concentration–voltage diagrams. Figure 2 shows the calculated $N_D - N_A$ versus applied bias voltage of each MIS structure near the flat band voltages (from −5 V to + 5 V).

The applied dc voltage is interrelated with the depletion width of the MIS structure. For the negative voltages a constant

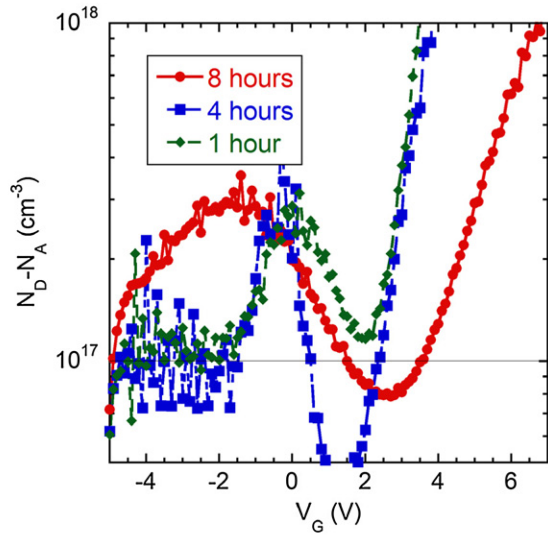

Figure 2. Net donor concentration vs. the applied DC voltage. $N_D - N_A$ was calculated from the CV curves of each MIS structure using equation (1).

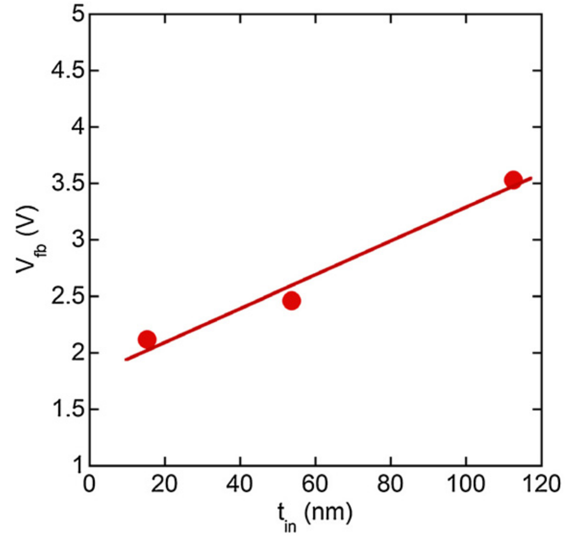

Figure 3. Flat band voltage data (red dots) as a function of the insulator thickness. V_{fb} increases with the insulator thickness t_{in}.

net donor concentration of approximately 1×10^{17} cm^{-3} is measured, which is attributed to the background donor concentration of the unintentionally doped (UID) cubic GaN. This residual background carrier concentration is the same for all our samples and is indicated in figure 2 by the gray horizontal line. For a direct estimation of the flat band voltage V_{fb} we plot the donor concentration versus the applied dc voltage instead of the depletion depth. In this way the exponential increase of $N_D - N_A$ in the strong accumulation regime at positive bias can be used to determine the flat band voltage from the intercept point of the measured curves with the gray line, which corresponds to the background doping in the semiconductor. In addition, at approximately 0 V, an additional charge accumulation is detected with a maximum of charge carriers of about 3×10^{17} cm^{-3}, which may be due to defect states at the surface of c-GaN.

Figure 3 shows the evaluated flat band voltage V_{fb} as a function of the insulator thickness t_{in}. The shift of the flat band voltage is a clear indication of charges in the insulator. The experimental V_{fb} versus t_{in} data points plotted in figure 3 show an increase of the flat band voltage with the insulator thickness.

We use energy band diagram analysis to understand the physical properties of the interface. Figure 4 shows a qualitative conduction band diagram of the MIS capacitors with different oxide thicknesses under the flat band condition.

V_g is the flat band gate bias for each thickness t_{in}, ϕ_b is the barrier height at the Ni/Si_3N_4 interface, F_{in} is the electric field in the silicon nitride layer, ΔE_c is the conduction band discontinuity between Si_3N_4 and c-GaN, and ψ is the energy separation of the conduction band from the Fermi level in the cubic GaN layer. Assuming an interfacial charge at the Si_3N_4/c-GaN interface, a simple analytical expression relating the applied flat band voltage to the interfacial parameters can be derived from figure 4:

$$qV_{\text{fb}} = qF_{\text{in}}t_{\text{in}} + (\phi b - \Delta E_C - \psi)\,. \qquad (2)$$

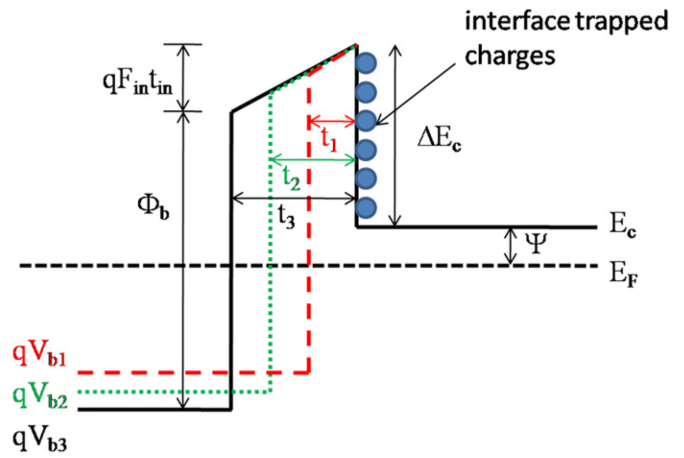

Figure 4. Schematic drawing of the conduction band alignment of a Ni/Si_3N_4/c-GaN metal insulator semiconductor structure with different insulator thickness. For a better overview the energy separation of the conduction band and the Fermi level Ψ is just shown for the structure with the insulator thickness t_3 (black full curve).

V_{fb} is the flat band voltage for the given insulator thickness t_{in}. Assuming a fixed interface trapped charge and a linear increase of the flat band voltage with the insulator thickness (figure 3), the electric field dropping across the insulator under the flat band condition is 0.148 MV cm^{-1} and the $(\phi_b - \Delta E_C - \psi)$ band offset is 1.807 eV. The nonzero electric field dropping across the Si_3N_4 insulation layer can be attributed to a net negative charge at the Si_3N_4/c-GaN interface, of approximately 6.1×10^{11} cm^{-2}. Based on the doping density, the conduction band distance from the Fermi level ψ is estimated to be 75.9 meV. Assuming a work function of 5.15 eV for Ni [10] and an electron affinity of 2.1 eV for Si_3N_4 [11], the barrier height at the Ni/Si_3N_4 interface is 3.05 eV. We find a conduction band discontinuity $\Delta E_C =$ 1.17 eV. This value is slightly lower compared to the value of 1.3 eV for hexagonal GaN reported in reference [11].

A very sensitive technique for characterizing insulator–semiconductor interface properties relies on characterizing the interface trap conductance by directly measuring the energy loss during capture and emission of the majority carriers (electrons) between conduction band and interface trap levels under the applied ac signal [6, 12, 13]. After series and insulator capacitance correction, the remaining parallel conductance G_p value includes only interface trap information. The equivalent parallel conductance G_p divided by ω is given by

$$\frac{G_p}{\omega} = \frac{C_{\mathrm{it}}\omega\tau_{\mathrm{it}}}{1+\omega^2\tau_{\mathrm{it}}^2} \tag{3}$$

where $\omega_{\mathrm{it}} = 2\pi f$ and τ_{it} is the interface trap lifetime [10]. At a given bias voltage, the plot of G_p/ω versus ω goes through a maximum when $\omega\tau_{\mathrm{it}} = 1$, and thus gives τ_{it}. The value of G_p/ω at the maximum is $C_{\mathrm{it}}/2$, where C_{it} is the capacity associated with the interface traps. Once C_{it} is known, the interface trap density is obtained by using the relationship

$$D_{\mathrm{it}} = \frac{C_{\mathrm{it}}}{q_{\mathrm{el}}A} \tag{4}$$

where A is the metal contact area and q_{el} is the single electron charge.

Figure 5(*a*) shows G_p/ω versus frequency curves measured at different bias voltages with a PECVD produced structure.

The peak shifts to higher frequencies at positive voltages between 5 V and 8 V indicating a continuous distribution of interface states within the band gap. Simultaneously the peak intensity increases. In figure 5(*b*) the G_p/ω versus ω curves of the MBE produced sample are shown. Nearly no shift of the maximum is observed in this sample. The interface trap density which is proportional to the peak height is 1 order of magnitude lower than that for the PECVD sample. The interface trap life time τ_{it} is given by the Shockley–Read–Hall model [14]:

$$\tau_{\mathrm{it}}\,(E_{\mathrm{it}}) = \frac{1}{\sigma_{0n}\upsilon_{\mathrm{th}}N_C}\exp\left(\frac{E_C - E_{\mathrm{it}}}{K_B T}\right) \tag{5}$$

where N_C is the effective density of states in the conduction band, υ_{th} is the thermal velocity of electrons, $\sigma_{0\mathrm{n}}$ is the capture cross section of the trap, E_C is the conduction band edge, E_{it} is the trap energy level below the conduction band edge, k_B is the Boltzmann constant and T is the temperature.

The frequency $\omega_{\max}$ at the maximum of G_p/ω gives $\tau_{\mathrm{it}} = 1/\omega_{\max}$ and correlates $\omega_{\max}$ with a corresponding trap energy level E_{it} below the conduction band edge. The thermal velocity and density of states are well known for a specific semiconductor, whereas the capture cross section of the traps depends strongly on the nature of the trap. The capture cross section can take values varying from 10^{-12} cm^2 to 10^{-18} cm^2 affecting the energetic position of the traps within the c-GaN bandgap. Since up to now this value is not known for cubic GaN, we assume in analogy to MBE grown GaAs an average capture cross section of 10^{-15} cm^2 [15] to convert τ_{it} into trap level energies. An aberration of the capture cross section value of ± 3 orders of magnitude results in a shift of the energetic position of ± 170 meV within the bandgap.

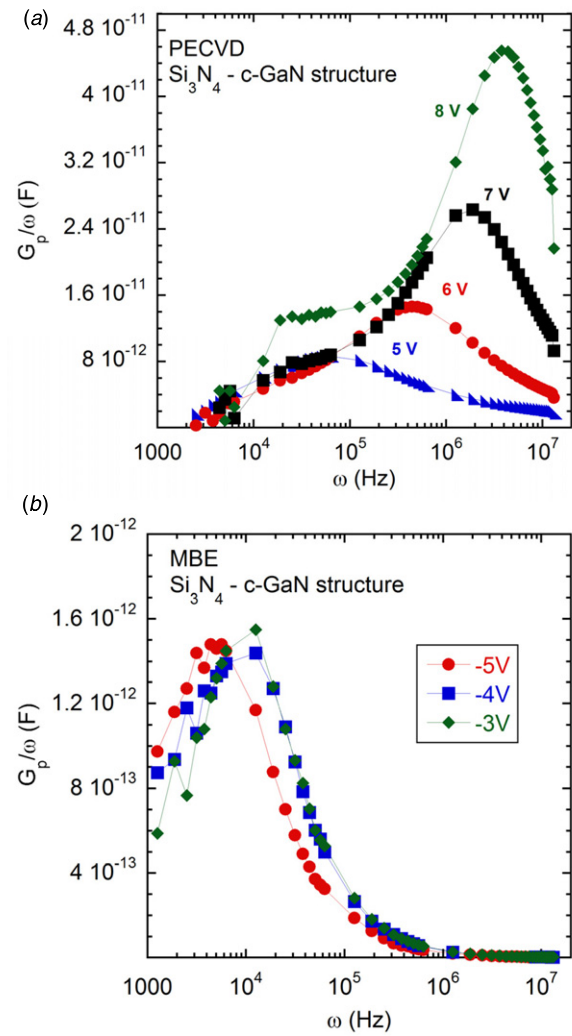

Figure 5. G_p/ω versus the angular frequency for the PECVD (figure 5(*a*)) and the MBE (figure 5(*b*)) samples. The peak maximum in the PECVD produced sample shifts to higher frequencies with positive voltage indicating a distribution of interface states. In contrast to this the peak maximum of the MBE-produced sample shows nearly no shift. The values for G_p/ω are 1 order of magnitude lower in the MBE produced structure.

In figure 6 we plot the obtained density of states of interface states D_{it} versus energy of the trap level within the gap of c-GaN.

An increase of $D_{\mathrm{it}}(E_{\mathrm{it}})$ with increasing energy is observed in structures with Si_3N_4 produced by PECVD, indicating a distribution of interface defect levels at about 0.3 eV below the conduction band with a maximum trap density of about 2×10^{12} cm^{-2}eV^{-1}. In structures with Si_3N_4 produced by plasma-assisted MBE, the trap states seem to have less energy spread. We find a maximum trap density of 2.5×10^{11} cm^{-2}eV^{-1} about 0.4 eV below the conduction band edge. Thus growth of Si_3N_4 under high vacuum conditions in the MBE chamber directly after the growth of cubic GaN reduces the interface trap density by more than 1 order of magnitude. Since the interface is not in contact with the atmosphere, the incorporation of impurities causing traps or mobile charges in the Si_3N_4 layer is significantly reduced. For comparison we have also included the energy distribution

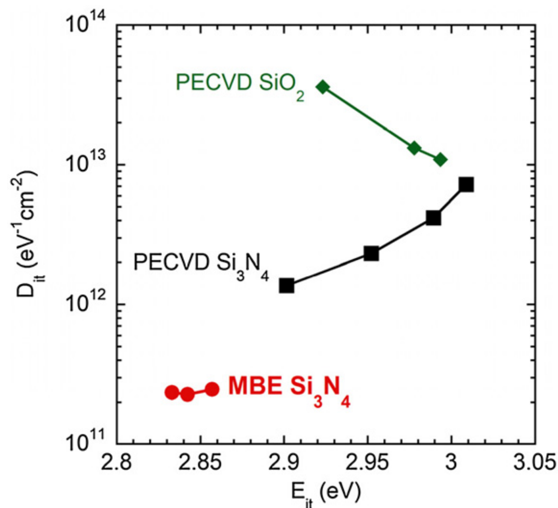

Figure 6. Interface state density D_{it} versus energy E_{it} within the band gap of c-GaN. The data from the MBE produced structure (red dots) are compared with PECVD produced Si_3N_4 (black squares) and SiO_2 (green diamonds) capacitors.

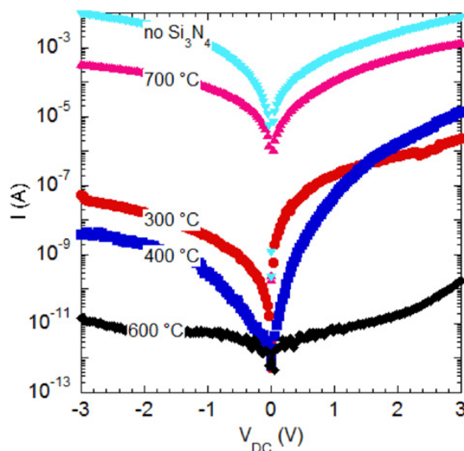

Figure 7. Current–voltage (IV) characteristics of the MIS capacitors with Si_3N_4 as insulator grown at different temperatures. To illustrate the effect of insulation the IV curve of a metal/semiconductor is also shown (no Si_3N_4).

of interface traps of SiO_2/c-GaN MIS structures [16] in figure 6. The interface trap density in these structures is in the range of 10^{13} cm^{-2} eV^{-1}, 2 orders of magnitude higher than that in Si_3N_4/c-GaN layers produced by the MBE method.

3.2. Influence of the growth temperature of the Si_3N_4 layers on their electric properties

In this section we discuss the influence of the substrate temperature during the deposition of the Si_3N_4 layers on their electrical properties. Five silicon nitride layers on top of c-GaN samples were grown at temperatures between 300 °C and 700 °C in 100 °C steps. The deposition duration was 1 h for each sample, so the Si_3N_4 layers have approximately the same thickness. In figure 7 current–voltage characteristics of the MIS capacitors are shown to illustrate the effect of insulation.

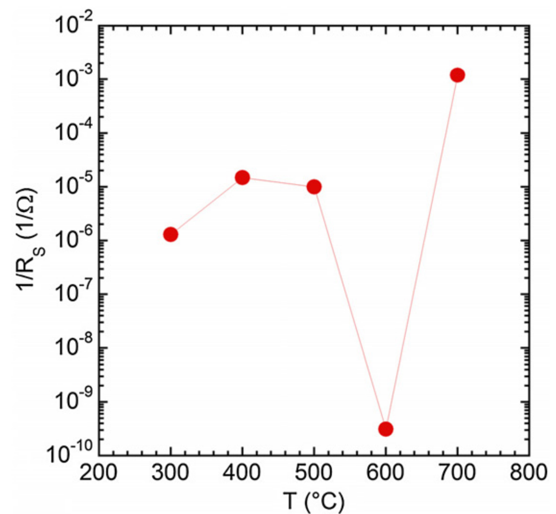

Figure 8. Calculated serial conductivity $1/R_S$ of the MIS capacitors. A minimum of conductivity is reached in the MIS structure grown at 600 °C.

A simple metal–semiconductor reference sample was also measured (no Si_3N_4). For positive bias voltages we observe a clear reduction of the current flow by 3 orders of magnitude for the MIS structures grown at 300 °C and at 400 °C compared to the reference sample. The sample grown at 600 °C shows a conductivity minimum. Within the measured voltage range the current is in the region of 10^{-10} A at +3 V. This value is more than 7 orders of magnitude lower as measured for the reference sample. The sample grown at 700 °C shows an insufficient insulation and the current is only a factor of 5 lower than that for the sample without an insulator at +3 V.

The current in reverse voltage direction also depends on the Si_3N_4 growth temperature and decreases with higher temperatures. In the sample grown at 600 °C the current is reduced to a minimum of 1.5×10^{-11} A at −3 V. The sample grown at 700 °C shows nearly the same conductivity as the reference sample. We assume that this is due to the high growth temperature, which is only 20 °C beneath the growth temperature of cubic GaN. Although the exact nature of this effect is still unknown, a diffusion of Si atoms into the c-GaN layer, acting as shallow donors, may explain the insufficient insulation and further investigations are underway. From the increase of the IV curves in forward direction the serial conductance $1/R_S$ was calculated. Figure 8 shows the results, with a clear conductivity minimum in the sample produced at 600 °C.

We performed two further investigations to understand the conductivity minimum in the MIS structure with Si_3N_4 grown at 600 °C.

In our first experiment time of flight secondary ion mass spectroscopy was performed. In figure 9 SIMS profiles of insulator c–GaN samples grown at 300 °C (figure 9(*a*)) and at 600 °C (figure 9(*b*)) are depicted.

The diagrams show the SIMS intensity plotted versus the sputtering time for oxygen (red dots), silicon nitride (blue squares) and the GaN signal (green diamonds). A silicon nitride layer was detected on top of the c-GaN layer. A noticeable incorporation of oxygen is measured in all samples.

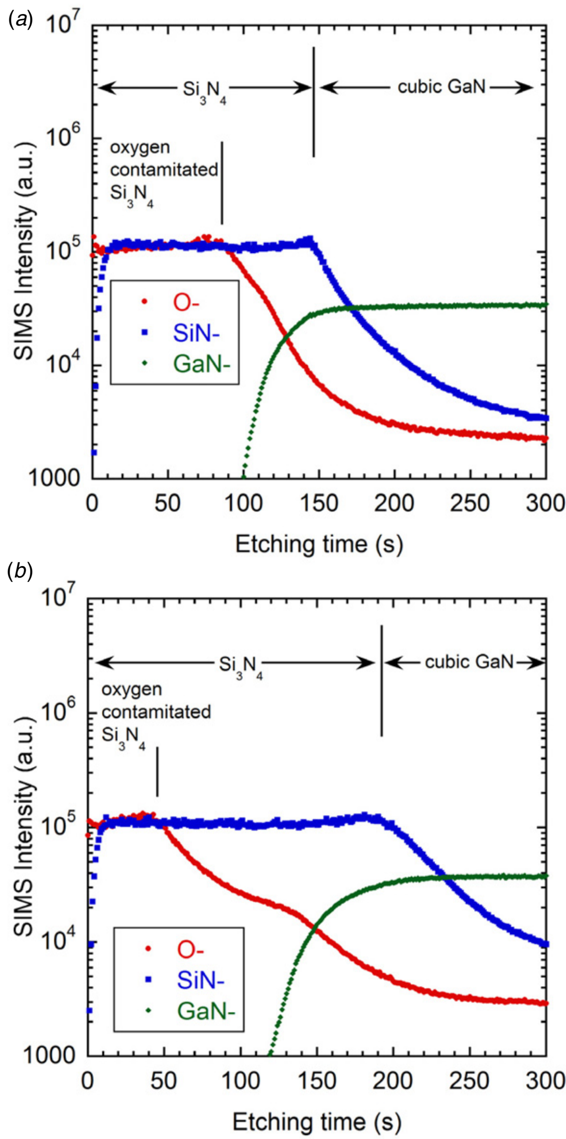

Figure 9. SIMS profiles of Si_3N_4/c-GaN structures, silicon nitride was grown at 300 °C (figure 9(a)) and at 600 °C (figure 9(*b*)). For a better overview only the signals for O (red curve), SiN (blue curve) and GaN (green) are shown.

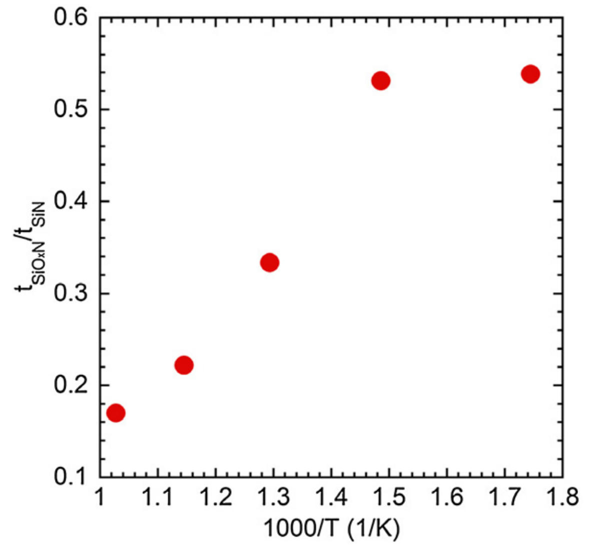

Figure 10. Fraction of oxygen-contaminated Si_3N_4 as a function of $1/T$. At temperatures between 400 °C and 600 °C a nearly linear regime with $1/T$ is observed.

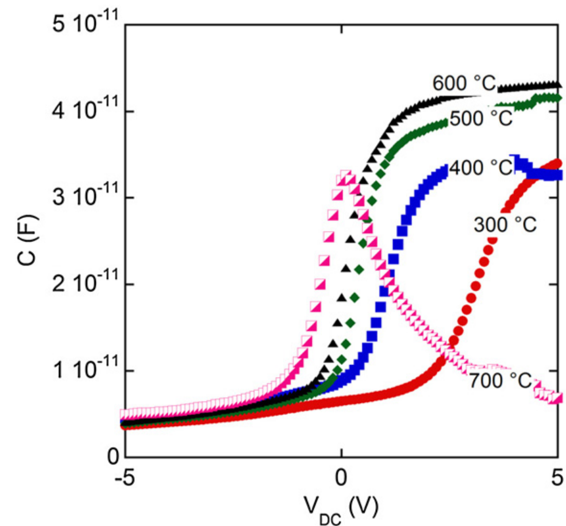

Figure 11. Capacitance–voltage (CV) characteristics of the MIS capacitors. The growth temperature for *in situ* MBE grown Si_3N_4 varied between 300 °C and 700 °C.

We believe that this oxide contamination is formed during the exposition of the samples to the atmosphere after the MBE growth process, since the oxygen incorporation in the c-GaN layer is more than 3 orders of magnitude lower than that in the Si_3N_4 layer. The oxygen contamination inside the c-GaN layer is due to residual oxygen in the nitrogen gas source, which is the same for the GaN growth and the Si_3N_4 growth. Since the nitrogen flux was not changed for Si_3N_4 and the growth rate between GaN and Si_3N_4 varies only by a factor of 10, we conclude that the oxide contamination does not originate from the growth process.

In the atmosphere SiO_2 or SiO_xN may be formed; the fraction of the oxygen-contaminated Si_3N_4 decreases at higher deposition temperatures and is a function of $1/T$ as illustrated in figure 10.

We suppose that the oxygen contamination is due to the formation of SiO_2 and SiO_xN on the Si_3N_4 layers, so with higher temperatures the porosity may decrease minimizing the oxide contamination and also the leakage current through the insulator. However this approach does not explain the increase of the conductivity in the sample grown at 700 °C.

In a second step we investigate the flat band condition in the grown samples. As discussed in section 3.1 the nonzero electric field dropping across the insulator is caused either by charges inside the insulator or by interface trapped charges at the Si_3N_4/c-GaN interface. To improve the insulating properties of the Si_3N_4 layer this parasitic charge should be reduced to a minimum. A hint of the reduction of these charges is a decrease of the flat band voltage. Figure 11 shows the CV characteristics of the samples which were reported in the IV analysis above (figure 7).

A drop of the capacitance at zero bias is observed for the sample grown at 700 °C indicating that the ohmic regime

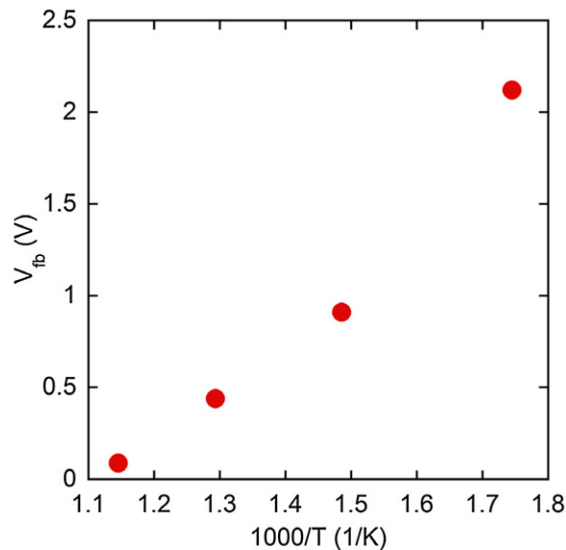

Figure 12. Extracted values for the flat band voltages of the MIS capacitors as a function of the reverse growth temperature.

becomes dominant in this structure at positive voltages. This observation fits very well with the high current in this sample (see figure 7). The samples grown at 300 °C and 400 °C show a slightly lower accumulation capacitance than the samples grown at 500 °C and 600 °C indicating a different insulator thickness. The Si_3N_4 thickness was calculated to be approximately 14 nm for the low-temperature samples and 12 nm for higher temperatures. As reported in section 3.1 of our discussion the flat band voltage was extracted from $N_D - N_A$ versus applied voltage profiles. The flat band voltage decreases with increasing growth temperature and reaches a minimum in the sample grown at 600 °C. In figure 12 the measured flat band voltage is plotted as a function of the inverse growth temperature (red circles).

A nearly linear behavior of V_{fb} versus $1/T$ with a high degree of correlation is observed. Summarizing these results the flat band voltage is reduced to a minimum for Si_3N_4 grown at 600 °C. The consequence is the reduction of the nonzero electric field across the insulator. This may cause the outstanding insulation properties of this layer.

4. Summary

We have fabricated metal–insulator–semiconductor structures with nonpolar cubic GaN deposited on highly conductive 3C–SiC (0 0 1) substrates. The trap energy and trap densities in MIS structures produced *in situ* by molecular beam epitaxy and *ex situ* by plasma-enhanced chemical vapor deposition are compared. From detailed band structure analysis the conduction band discontinuity between Si_3N_4 and cubic GaN was estimated to be 1.17 eV and is slightly lower than the literature value of 1.3 eV for hexagonal GaN. By admittance spectroscopy interface traps were detected between 0.2 eV and 0.4 eV below the conduction band edge. A minimum of interface defect density of $D_{it} = 2.5 \times 10^{11}$ cm^{-2} eV^{-1} was estimated for Si_3N_4/c-GaN structures grown by MBE. This value is 1 order of magnitude lower than that in the PECVD produced Si_3N_4 structure and 2 orders of magnitude lower than that measured with SiO_2 insulator layers. A minimum of conductivity was measured by current–voltage analysis in the sample grown at 600 °C. Our results demonstrate that MBE produced *in situ* Si_3N_4 layers have a great potential as gate dielectrics in MIS structures on c-GaN with outstandingly insulating properties and low interface trap density.

Acknowledgments

The project was financially supported by the German Science Foundation (DFG, project As 107/4-1). H Nagasawa, HOYA Corporation, SiC Development Center, Japan is acknowledged for the supply of the 3C–SiC substrates. K Lischka is acknowledged for helpful discussions.

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