three heaters were driven by the same electric power. Fig. 2 shows the fibre-to-fibre transmission of the selected (ON) and other (OFF) ports as a function of the total applied power. When no electric power was supplied to any of the heaters, the 1 × 8 TO switch functioned as a splitter with an insertion loss of 11.5 – 12.5dB. At driving powers of 390–450mW, the insertion loss was < 2.9dB and the crosstalk was < –41dB. Since the waveguide propagation loss was 2.0dB and the fibre coupling loss was ~0.1dB, we estimated the excess loss for each component switch to be 0.3dB. We tested all the switched states of the 1 × 8 switch chip at a driving power of 450mW. The insertion loss for the worst state was 3.0dB and the worst crosstalk value was –40dB. This loss value is the lowest yet reported for polymeric 1 × 8 optical switches. The polarisation dependent loss was < 0.1dB for the ON output and ~3dB for the OFF output. The rise and fall times were 6 and 3.4ms, respectively. These values agree with the response time for simulated thermal diffusion.

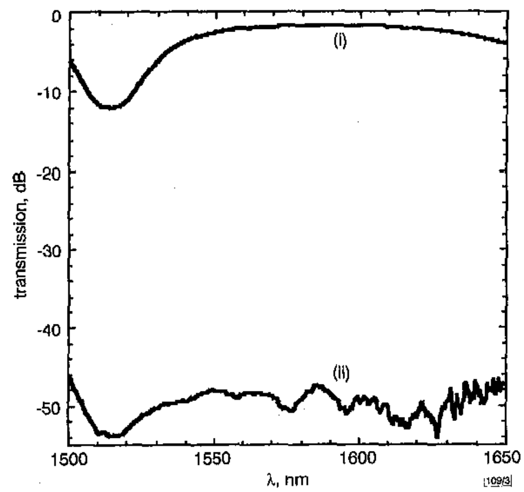

Fig. 3 *Fibre-to-fibre transmission spectra of 1 × 8 digital optical switch at 390mW driving power*

(i) ON port
(ii) OFF ports

Fig. 3 shows the transmission spectra of the ON and OFF ports. We achieved a low insertion loss of < 4dB in the 1540–1650nm wavelength band, which covers both conventional and gain-shifted EDFA bands.

Conclusion: We have demonstrated a 1 × 8 digital TO switch which uses silicone resin waveguides. We designed our compact 40 mm long switch using short Y-branching switches with a large branching angle. The switch had a low insertion loss of < 3dB and a low crosstalk of < –40dB at 1550nm. These excellent characteristics meet the requirements for optical components in advanced optical cross-connect systems.

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Optical polarisation-mode dispersion compensation of 2.4bit durations of differential group delay at 40Gbit/s

D. Sandel, S. Hinz, M. Yoshida-Dierolf, R. Noé, R. Wessel and H. Suche

A method for realising the optical polarisation-mode compensation of a differential group delay of 2.4bit durations is demonstrated for the first time, using a distributed fibre optic equaliser. As a result, it is believed that much of the existing fibre network can be upgraded even to 40Gbit/s and RZ signal format.

Motivation: Polarisation-mode dispersion (PMD), especially in installed fibre, broadens optical pulses in a time-variant manner and therefore impedes the development of highest-capacity, long-haul communication systems.

It is commonly believed that, if any method for reducing PMD other than regeneration can be found, it will be limited to first-order differential group delays (DGDs) of the order of one bit duration. This is certainly true for compensators with just one [1 – 4] or a few [5] DGD sections and polarisation transformers. However, distributed equalisers with mode converters embedded in a birefringent waveguide [6, 7] are less restricted in this respect because a larger number of polarisation transformers can be implemented without introducing significant loss or cost.

While the best previously reported result for compensated DGD was 1.7bit durations at 20Gbit/s [6] we report here the compensation of DGD of 2.4bit durations at 40Gbit/s using RZ signals. This is challenging because the compensator must have at least the DGD to be compensated, thereby raising the total DGD to > 5 bit durations in our case. On the other hand it is rewarding because 1.4 times more tolerable DGD means that the transmission fibre may be twice as long.

Compensator: A ~320m long polarisation-maintaining fibre with a large beat length of Λ = 23mm was pulled through the hollow axes of 64 stepper motors, grouped as 32 pairs along the fibre [6]. The total compensatory power was 77ps DGD. Each twister pair can convert a horizontal principal state-of-polarisation to half its amount into its orthogonal, with an endlessly adjustable coupling phase. The fibre twist angles α_1, α_2 needed to perform this operation are shown in Fig. 1. Smaller twist angles correspond to less mode coupling.

With at least half mode coupling accessible in each twister pair the equaliser is able to bend these 'joints' of its DGD profile (i.e. the concatenation of PMD vectors) by ≥ 90° in any direction in the three-dimensional space of normalised Stokes vectors.

Transmission system: The system (Fig. 2) was similar to that described in [7]. A 10GHz modelocked Ti:Er:$LiNbO_3$ waveguide laser (MLL) produced 5.9ps (FWHM) pulses at λ = 1561nm which were subsequently modulated at 10Gbit/s. The data signal was optically multiplexed to 40Gbit/s. A PMD emulator was used to simulate a transmission fibre. It consisted of a 40 and a 20ps DGD piece of polarisation-maintaining fibre (PMF), preceded, separated and followed by a total of eight motorised fibre loop devices (λ/4, λ/2, λ/4 groups). The PMD was compensated for in the fibre optic 77ps equaliser.

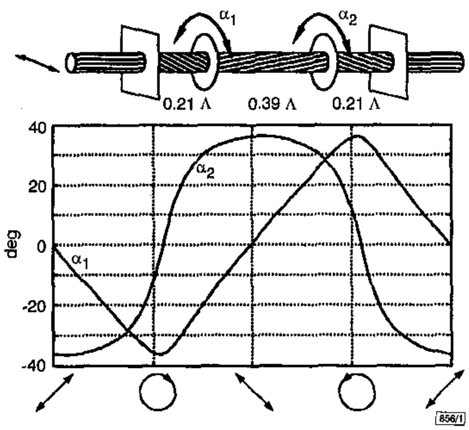

Fig. 1 *Twist angle pairs needed for different output polarisations corresponding to half mode conversion of horizontal input polarisation*

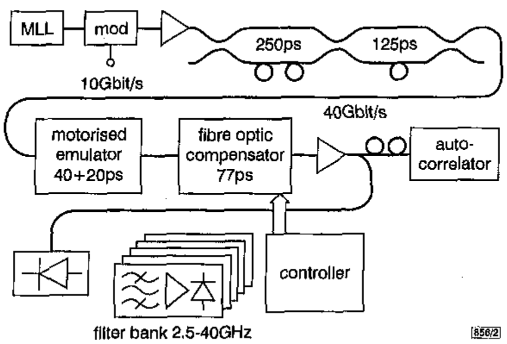

Fig. 2 *Experimental setup*

At the receive end the signal was detected in a 40GHz photodiode. The electrical signal was amplified and then analysed in a filter bank which contained five bandpass filters with centre frequencies ranging from 2.5 to 40GHz. The 40GHz filter was a spectrum analyser tuned to the clock line. The lowpass-filtered signals were read into a PC which worked as a controller.

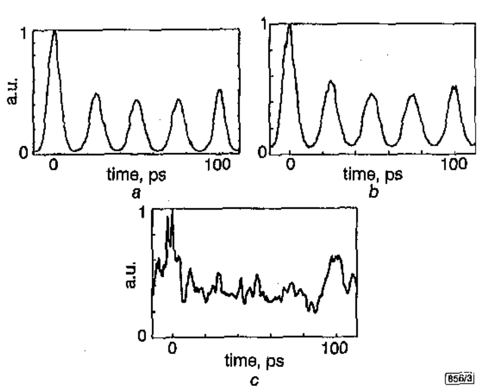

Fig. 3 *Autocorrelation traces*

a Back-to-back, 5.9ps
b With emulator and compensator, 6.6ps
c Worst case

Experiment: An SHG autocorrelator monitored the received pulsewidth. Although polarisation-dependent and slow, it is still useful for measuring static PMD. Fig. 3*a* shows the centre and one half of the back-to-back autocorrelation trace, consistent with 40Gbit/s, 5.9ps RZ pulses. As a next step the PMD emulator and the compensator were inserted, and control was switched on. Now the autocorrelation trace indicated marginal pulse broadening to a deconvolved 6.6ps width, together with a slightly increased pedestal (Fig. 3*b*). For comparison we also give an autocorrelation trace for the emulator plus compensator when the controller was made to minimise rather than maximise the signal quality. In this case the original pulses essentially disappear due to PMD (Fig. 3*c*).

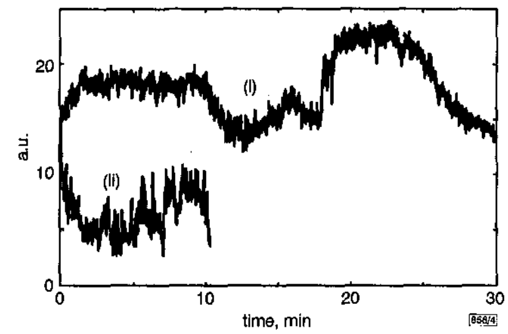

Fig. 4 *Eye opening equivalent signal recorded while emulator is varied*

(i) Control active
(ii) Control disabled

A dynamic measurement was made with the 40 + 20ps emulator and the compensator. The motorised fibre polarisation transformers were made to turn, each at a different speed and with alternating directions. Fig. 4(i) shows an aggregate control signal obtained from the filter bank. It reflects, probably even in a pessimistic manner, the eye opening to be expected in a digital receiver. Part of the signal variations can be attributed to the polarisation dependence (~ 1dB optical ⇒ ~ 2dB electrical) of the components following the compensator. Control was then stopped while the emulator coils continued to turn. The aggregate control signal varied at a substantially lower level (Fig. 4(ii)).

The present experiment shows that 60 ps of DGD can be equalised at 40Gbit/s. Distributed PMD compensators in X-cut, Y-propagation Ti:$LiNbO_3$ [7] have a much faster response and should make possible the cost-effective upgrade of most existing fibres to 40Gbit/s.

Conclusions: A distributed fibre optic polarisation-mode dispersion equaliser has been used to compensate for a differential group delay of 2.4 bit durations, which is the highest reported value to our knowledge. The data rate was 40Gbit/s, and the 5.9ps RZ pulses were broadened only to 6.6ps.

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Parallel FEC code in high-speed optical transmission systems

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Parallel FEC code transmission is proposed, in which check bits are transmitted on a different wavelength. The signal format is perfectly compatible with SDH in terms of signal wavelength. A smooth upgrade to the FEC system is possible by connecting additional modules. High FEC capability is obtained such that the BER of 10^{-6} can be improved to 10^{-11} with a decoding delay of several bits. When the parallel processing number is 8, the GVD tolerance is extended by a factor of 2.5, while the number of L-REPs possible in an optical link is doubled.

Introduction: In high-speed long-distance optical transmission systems faster than 2.5Gbit/s several transmission degradations need to be overcome, such as the group velocity dispersion (GVD) of the fibre used and the amplified spontaneous emission (ASE) noise accumulation of linear repeaters (L-REPs) employing erbium-doped fibre amplifiers (EDFAs). The use of forward error correcting (FEC) codes offers the potential to improve these degradations in the electronic regime. One area of interest is that network node interfaces are being standardised around the synchronous digital hierarchy (SDH), which includes section overhead (SOH) bits for network operation purposes. As the networks are being widely or globally deployed, international or inter-carrier connections based on standardised interfaces are becoming more important. So far, three kinds of FEC code compatible with SDH have been proposed [1 – 3], e.g. the so-called 'in-band FEC'. However, all of them utilise unused overhead (OH) fields for check bit insertion, which results in limited error correcting capability due to the restricted bandwidth available for check bits. Simpler circuits are desirable for high-speed transmission systems. If a multiple (complex) FEC code is selected, then the error location algorithm at the decoder will be a bottleneck in the system. In addition, if the FEC circuit encodes data in a serial manner, data should be stored in memories of the decoder: therefore, the operational speed of the memories (up to 100MHz) will be another bottleneck in the system. An interesting development is product-coded wavelength division multiplexing (WDM) [4], where data are encoded in a fully parallel manner by a simple single error correcting (SEC) code. However, the delay differences among the many wavelengths caused by GVD are difficult to offset, which limits the transmission distance. Delay differences over long distances could be suppressed if the wavelengths are in the vicinity of the fibre's zero-dispersion wavelength. However, more than three wavelengths yields four wave mixing (FWM) induced crosstalk, and an SEC code will fail to overcome this significant degradation. In this Letter we basically propose a two wavelength parallel FEC code which assigns another wavelength to carry check bits. The proposed FEC code leads to both high FEC capability and perfect SDH compatibility with respect to the signal wavelength. Phase adjustment is necessary only between two wavelengths. In addition, WDM long-haul transmission can be obtained by avoiding the FWM effect using nonzero dispersion-shifted fibre (NZDF) and by multiplexing the pairs of wavelengths; signal and check bits. The proposed FEC code will be also effective on nonlinear optical effects such as self-phase modulation (SPM) [3] or cross-phase modulation (XPM).

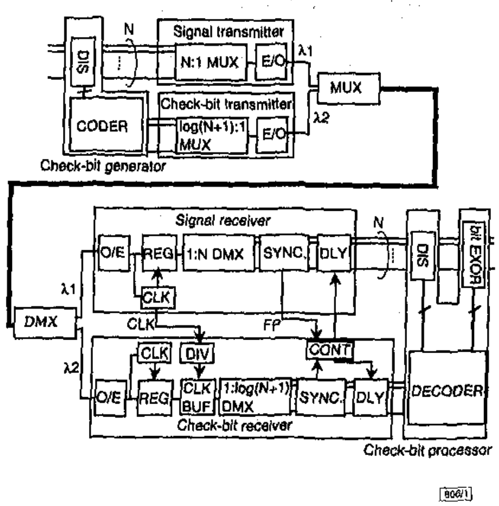

Fig. 1 *Proposed system configuration*

Table 1: Generator polynomials and shortened polynomials

Parallel number	Generator polynomial $g(x)$	Shortened polynomial $h(x)$
8	$x^4 + x + 1$	$x^3 + x + 1$
16	$x^5 + x^2 + 1$	$x^4 + x^3 + x^2 + x + 1$
32	$x^6 + x + 1$	$x^5 + x^2 + 1$
64	$x^7 + x^3 + 1$	$x^3 + x$

System configuration: Fig. 1 shows the proposed system configuration. The system consists of a signal transmitter/receiver, check bit transmitter/receiver, check bit generator/processor, and optical multiplexer/demultiplexer (MUX/DMX). The module configurations realise smooth upgrading from a non-FEC system to an FEC system, by adding a check bit transmitter/receiver and check bit generator/processor to the SDH system. Signal processing such as frame synchronisation is executed in an N-parallel manner. The proposed scheme performs Hamming coding on the N-parallel bit block as a message, therefore $\log(N+1)$ check bits are required. The signal transmitter consists of an N:1 bit-MUX and E/O of wavelength λ1, the check bit transmitter includes a $\log(N+1)$:1 bit-MUX and an E/O of wavelength λ2, while the check bit generator contains distributor and encoder circuits which perform division on the signal stream with respect to the generator polynomial $g(x)$ with multiplication for the shortened polynomial $h(x)$. Table 1 lists the parallel numbers N, generator polynomials $g(x)$ and shortened polynomials $h(x)$. The signal receiver consists of an O/E, clock recovery circuit (CLK), regenerating circuit (REG), 1:N bit-DMX, frame synchronisation circuit (SYNC), and variable phase shifter (DLY). The phase is adjusted either manually at system startup or automatically using check-bit receiver feedback. In the case of large delay differences, a fibre delay line will be placed in front of the O/E. Fibre length adjustment is simple because only two wavelengths are considered even in WDM systems. The check bit receiver includes a 1:$\log(N+1)$ bit-DMX, frequency divider (DIV), clock buffer (CLK BUF) for bit synchronisation, SYNC for check bits, and an additional controller for phase adjustment of the frame synchronisation pulses (automatic control version). The check bit processing circuit contains a distributor, FEC code decoder, and bit-based exclusive-or (bit EXOR).